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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,174	03/16/2004	Bernd Barchmann	E0196.0005	4131

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DICKSTEIN SHAPIRO LLP
1177 AVENUE OF THE AMERICAS 6TH AVENUE
NEW YORK, NY 10036-2714

EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,174	BARCHMANN ET AL.	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *14-17 and 25-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-13,18-24 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 pg*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Specie III (figures 7-9, third embodiment), claims 1-13, 18-24, and 30-33, in the reply filed on 5/12/06 is acknowledged. The traversal is on the ground(s) that Specie IV is actually part of Specie I, Specie II is just a variation of Species I, and Species III is just an extension of Species I. This is not found persuasive because each specie has a different structure (1st-4th embodiments) as disclosed in the specification (pages 9-10) and in the drawings. The requirement is still deemed proper and is therefore made **FINAL**. Claims 1-13, 18-24, and 30-33 are treated on the merits in this Office Action.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the spacer (see claim 24) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claim contains the Trademark "ISO". This term should be replaced with the generic term for the metallization.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-13, 18-24, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huber et al. (US 6384425) in view of Kawan (US 6235553).

Regarding claim 1, as shown in figures 1-2, Huber discloses a nonconducting substrate 2 (col.3:36) forming a strip 1 (col.3:33) on which a plurality of carrier elements having respective boundary lines 4 (contour lines, col.3:51) are formed, comprising:

(a) A contact side (no number, as shown in figure 1);

(b) an insertion side (no number, as shown in figure 2);

(c) a conducting insertion-side metallization 9/10/11/14/15 (conductor, col.3:62) provided on the insertion side.

But, Huber does not disclose the insertion-side metallization is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization. Indeed, Huber discloses the insertion-side metallization is formed for wire bonding instead. However, flip-chip technology is old and known in the art; therefore, it is only a mater of design choice depending upon particular applications by rearranging contact points for flip-chip connections.

Kawan, as shown in figures 7-10, discloses a flip-chip technology for inserting a semiconductor chip on an insertion side of a smart card comprising a contact side and an insertion side (front side/rear side, figures 2-3, col.3:49-60), a conducting insertion-side metallization 52-59 (bonding points, col.6:55) provided on the insertion side. Wherein the insertion-side metallization 52-59 is formed such that an electrical connection can take place by means of flip-chip bonding between contact points of an integrated circuit to be applied to the insertion side and the insertion-side metallization (col.6:48-col.8:65).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings about the flip-chip from Kawan on the carrier elements of Huber in order extend the capability of the carrier elements for a specific application to include flip-chip technology, which is widely in use in the industry, and to save cost in assembling because wire connections can be skipped.

Regarding claim 2, as shown in figure 2, Huber further discloses a plurality of contact elements 10/11 (col.4:2 and col.4:15) provided within each boundary line 4.

It is noticed that the limitation "at least partly for bonding flip-chip contacts of the integrated circuit" is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claim 3, as shown in figure 1, Huber further discloses a contact-side metallization 8 (metal lines, col.3:56) provided on of the contact side of the substrate.

Regarding claim 4, as shown in figure 1, Huber further discloses a plurality of contact areas 5 (contact surfaces, col.3:53-54), which are electrically isolated from one another and are provided on the contact-side metallization within each boundary line 4 (outer contour line, col.3:52).

Regarding claim 5, the limitation "the contact areas of the contact-side metallization are formed as ISO contact areas" is regarded as process claim limitation in a product claim and is treated in accordance with MPEP 2113. As this process limitation results in a product structure that is the same as the product of Nakamura et al., therefore Huber anticipates the claim.

Regarding claim 6, as shown in figure 2, Huber further discloses a plurality of contact elements 10/11 (col.4:2 and col.4:15) provided on the insertion-side metallization within each boundary line 4, wherein the contact areas of the contact-side metallization have at least partly an electrical connection with the contact elements of the insertion-side metallization (in order to test the semiconductor chip, see cut outs 12-13, col.3:64-col.4:15).

It is noticed that the limitation "at least partly for bonding flip-chip contacts of the integrated circuit" is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claim 7, as shown in figure 2, Huber further discloses the electrical connection, which is established by plated-through holes 12-13 (col.3:64-col.4:15 and col.5:13) extending through the substrate.

Regarding claim 8, as shown in figures 1-2, Huber discloses the plated-through holes that are each arranged in a plated-through region (arbitrary selected areas within the metal contact areas 5) of the contact areas of the contact-side metallization that is inherently not intended for bonding with an external reader.

Regarding claim 9, as shown in figures 1-2, Huber further discloses a boundary line region 4, which includes the contact-side metallization 5 and inherently brings about an increased moment of resistance in a region of the integrated circuit.

Regarding claim 10, as shown in figures 1-2, Huber discloses the boundary line region crosses a line of symmetry (considering a line dividing the area within the

boundary 4 in haft), which is formed between oppositely lying contact areas of the contact-side metallization.

Regarding claim 11, as shown in figure 2, Huber discloses the contact elements of the insertion-side metallization that are in a form of interconnects (as shown in the figure), which respectively have a first end and a second end (all conducting elements have first and second ends, wherein first and second ends are arbitrary defined).

Regarding claim 12, as shown in figure 2, Huber discloses the contact elements of the insertion-side metallization that are in a form of interconnects (as shown in the figure), which respectively have a first end and a second end (all conducting elements have first and second ends, wherein first and second ends are arbitrary defined), the first end (arbitrarily selected contact area around the cut-out 13 as a first end) of the interconnects overlapping with a respective one of the plated-through holes 13 and being in electrical connection therewith.

Regarding claim 13, as shown in figure 2, Huber in view of Kawan, discloses the second end (arbitrarily selected contact area 11 as a second end) has a first contact area 11 for the electrical bonding with a flip-chip contact of the integrated circuit.

Regarding claim 18, as shown in figure 2, Huber discloses at least some of interconnects 15 (col.3:62) are provided with area-covering metallizations (considering all metalized areas), which inherently serve for increasing the bending rigidity of the substrate.

Regarding claim 19, as shown in figure 2, Huber discloses the area-covering metallizations are formed within the boundary line 4 of the respective carrier element.

Regarding claim 20, as shown in figure 2, Huber discloses the area-covering metallizations are provided in a region outside the integrated circuit to be applied.

Regarding claim 21, as shown in figure 1, Huber discloses indexing holes 3 (perforations, col.3:41), which are provided on the substrate, and inherently to stiffen the substrate, are surrounded by metallizations 8 (col.3:55) on the insertion side and/or the contact side.

Regarding claim 22, as shown in figure 2, Huber discloses adjusting marks (no number, considering the bar connecting index holes 3 as an adjusting mask), which constitute part of the insertion-side metallization and are provided on the substrate for orientation of placement machines.

Regarding claim 23, as shown in figure 2, Huber further discloses transverse webs 8 (considering line 8 which runs in between left and right carrier elements) which constitute part of the insertion-side metallization and are provided on the substrate between neighboring carrier elements.

Regarding claim 24, Huber in view of Kawan discloses in a region of the integrated circuit to be applied, the insertion-side metallization inherently comprises spacers (formed by solder balls that electrically connecting a semiconductor chip and the insertion side metallization), which inherently ensure plane-parallelism between the integrated circuit and the insertion side of the substrate.

Regarding claim 30, Huber discloses the substrate 2 (col.3:36) consisting of glass fiber-reinforced epoxy resin (a thermoplastic resin), which is PEN.

Regarding claim 31, Huber discloses every limitation as shown in claim 30 above, but does not disclose the thickness of the substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select a thickness of the substrate to be within 50 to 125 .mu.m for a specific application, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 32, the limitation "the contact-side metallization and the insertion-side metallization are produced by a growing-on process" is regarded as process claim limitation in a product claim and is treated in accordance with MPEP 2113. As this process limitation results in a product structure that is the same as the product of Nakamura et al., therefore Huber anticipates the claim.

Regarding claim 33, Huber does not disclose the thickness of the contact-side metallization and the insertion-side metallization.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to select a thickness of the contact-side metallization and the insertion-side metallization to be less than 40 mu.m for a specific application, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Citation of Relevant Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Shrauger (US 6558976) discloses a critically aligned optical MEMS dies for large packaged substrate arrays and method of manufacture.

Corisis (US 6505400) discloses a method of making chip scale package with heat spreader.

McHugh et al. (US 5715143) disclose a carrier system for integrated circuit carrier assemblies.

Nakashima et al. (US 5661086) disclose a Process for manufacturing a plurality of strip lead frame semiconductor devices.

Yumoto et al. (US 5384204) disclose a Tape automated bonding in semiconductor technique.

Crane et al. (US 3838984) disclose a flexible carrier and interconnect for uncased IC chips.

Haghiri-Tehrani (US 5055913) discloses a terminal arrangement for integrated circuit device.

Jung et al. (US 4812421) disclose a tab-type semiconductor process.

Houdeau et al. (US 6288904) disclose a chip module, in particular for implantation in a smart card body.

Sumi (US 6992372) disclose a film carrier tape for mounting electronic devices thereon.

Cho (US 6914196) discloses a Reel-deployed printed circuit board

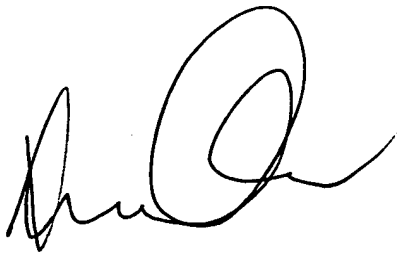
Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoa C. Nguyen
6/19/06



KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800